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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/611,948 | 07/03/2003 | Hisashi Ishikawa | 00862.023127. | 5415 |

5514 7590 06/04/2008

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| EXAMINER | |
|---|---|
| VO, QUANG N | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2625 | |

| MAIL DATE | DELIVERY MODE |
|---|---|
| 06/04/2008 | PAPER |

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/611,948 | ISHIKAWA, HISASHI | |
| | Examiner | Art Unit | |
| | QUANG N. VO | 2625 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *28 April 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1,3-7,20,22-26 and 39* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-7,20,22-26 and 39* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *4/28/08*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

**DETAILED ACTION**

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 04/28/2008 has been entered.

***Response to Amendment***

With regard to claim 1, applicant argues that Katayama does not discloses a bit connection component (step) that connects a decimal portion of image data of a preceding pixel to image data of a target pixel as lower bits of the image data of the target pixel, a correction component (step) that generates corrected image data by adding a correction value to the bit-connected image data of the target pixel, and a quantization component (step) that quantizes an integral portion of the corrected image data.

In response: Katayama disclose a bit connection component (step) (e.g., a program storing in the ROM 912 for executing adding pixel data to error data (a bit connection), block S3, figure 28, column 20, lines 4-6) that connects a decimal portion (e.g., a distribution-error value (decimal portion), column 20, lines 36-37) of image data of a preceding pixel (e.g., objective pixel, column 20, lines 44-46) to image data of a target pixel (e.g., a neighboring pixel (a target pixel), column 20, lines 44-48) as lower bits of the image data of the target pixel (e.g., error added to lower bits of neighboring

pixels, figure 27), a correction component (step) (e.g., data adding means block 902, error-to-be-distributed computing means block 903, and error storing means block 908, figure 25) that generates corrected image data (e.g., image outputting means block 909, figure 25) by adding a correction value to the bit-connected image data of the target pixel (e.g., data adding means 902 for adding an input image signal to an error distributed from neighboring pixels, column 19, lines 44-47), and a quantization component (step) (e.g., binarizing means block 903, figure 25) that quantizes an integral portion of the corrected image data (e.g., binarizing means 903 for binarizing a signal output from data adding means 902, figure 25, column 19, lines 47-49).

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 3, 7, 20, 22, 26, and 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Katayama et al. (Katayama) (US 5,488,673).

With regard to claim 1, Katayama discloses an image processing apparatus (e.g., an image processing apparatus, figure 26) comprising: a bit connection component (e.g., a program storing in the ROM 912 for executing adding pixel data to error data (a bit connection), block S3, figure 28, column 20, lines 4-6) that connects a decimal

portion (e.g., a distribution-error value (decimal portion), column 20, lines 36-37) of image data of a preceding pixel (e.g., objective pixel, column 20, lines 44-46) to image data of a target pixel (e.g., a neighboring pixel (a target pixel), column 20, lines 44-48) as lower bits of the image data (e.g., error added to lower bits of neighboring pixels, figure 27); a correction component (e.g., data adding means block 902, error-to-be-distributed computing means block 903, and error storing means block 908, figure 25) that generates corrected image data (e.g., image outputting means block 909, figure 25) by adding a correction value to the bit connected image data of the target pixel (e.g., data adding means 902 for adding an input image signal to an error distributed from neighboring pixels, column 19, lines 44-47); a quantization component (e.g., binarizing means block 903, figure 25) that quantizes an integral portion of the corrected image data (e.g., binarizing means 903 for binarizing a signal output from data adding means 902, figure 25, column 19, lines 47-49); a calculation component (e.g., arithmetic-error computing means block 905, figure 25) that calculates the quantization error, which is generated by quantization by quantization component (e.g., error distributing means (block 907) and error-to-be-distributed computing means (block 904), figure 25, column 19, lines 40-65); a buffer (e.g., error storing means (block 908), figure 25) that stores the calculated quantization error; and an error diffusion component (e.g., error storing means block 908 and data adding means block 902, figures 25) that generates the correction value to be added to input data of the next pixel by diffusing the quantization error stored in buffer (e.g., data adding means (block 902) for adding an input image signal to an error distributed from neighboring pixels, figure 25, column 19, lines 40-65).

Katayama differs from claim 1, in that he does not explicitly show a latch component that latches a decimal portion of the corrected image data to be connected to image data of a next pixel.

Katayama discloses in first embodiment a latch component that latches a decimal portion of the corrected image data (e.g., flip-flops 15a-15d for latching data, column 7, lines 31-36).

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to have modified Katayama's seventh embodiment to include a latch component that latches a decimal portion of the corrected image data as taught by Katayama's first embodiment. It would have been obvious to one of ordinary skill in the art at the time of the invention to have modified Katayama's seventh embodiment by the teaching of Katayama's first embodiment to distribute decimal portion back to image data to have better image.

With regard to claim 3, Katayama discloses further comprising a stop component that stops propagating the correction value in a case in which it is inappropriate to propagate the correction value to next and subsequent pixels (e.g., the error distribution controlling circuit, figures 6, column 7, line 61 – column 8, lines 63).

With regard to claim 7, Katayama discloses further comprising a numerical value limit component that limits the quantization error calculated by calculation component to a numerical value within a predetermined range (e.g., the error distribution controlling circuit, column 7, line 61 – column 8, line 65).

Referring to claim 20:

Claim 20 is the method claim corresponding to operation of the device in claim 1 with method steps corresponding directly to the function of device elements in claim 1. Therefore claim 20 is rejected as set forth above for claim 1.

Referring to claim 22:

Claim 22 is the method claim corresponding to operation of the device in claim 3 with method steps corresponding directly to the function of device elements in claim 3. Therefore claim 22 is rejected as set forth above for claim 3.

Referring to claim 26:

Claim 26 is the method claim corresponding to operation of the device in claim 7 with method steps corresponding directly to the function of device elements in claim 7. Therefore claim 26 is rejected as set forth above for claim 7.

Referring to claim 39:

Claim 39 is the computer-executable storage medium claim corresponding to operation of the device in claim 1 with instruction steps corresponding directly to the function of device elements in claim 1. Therefore claim 39 is rejected as set forth above for claim 1.

Claims 4-6, and 23-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Katayama et al. (Katayama) (US 5,488,673) as applied to claims 1 and 3 above, and further in view of Nakano et al. (Nakano) (US 6,977,756).

With regard to claim 4, Katayama differs from claim 4, in that he does not explicitly show a clear component to clear data/error portion in latch/temporary memory

in case in which it is inappropriate.

Nakano discloses a clear component to clear data/error portion in latch/temporary memory (e.g., it clears a content of the error holding register, column 5, lines 58-61).

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to have modified Katayama to include a clear component to clear data/error portion in latch/temporary memory in case in which it is inappropriate conditions as taught by Nakano. It would have been obvious to one of ordinary skill in the art at the time of the invention to have modified Katayama by the teaching of Nakano to clear data/error as needed.

With regard to claim 5, Nakano discloses further comprising a processing limit component that limits clearing by clear component when a scanning direction of the input image is reversed (e.g., adder 9 detects forward and reversed direction, column 9, lines 13-34).

With regard to claim 6, Nakano discloses wherein the case in which it is inappropriate to propagate the correction value to next and subsequent pixels includes at least one of a case in which a pixel of interest is a start pixel of a line, a case in which the pixel of interest has a value equal to a lower limit level of the input image, and a case in which the pixel of interest has a value equal to an upper limit level of the input image (column 8, line 48 – column 9, line 3).

Referring to claim 23:

Claim 23 is the method claim corresponding to operation of the device in claim 4 with method steps corresponding directly to the function of device elements in claim 4. Therefore claim 23 is rejected as set forth above for claim 4.

Referring to claim 24:

Claim 24 is the method claim corresponding to operation of the device in claim 5 with method steps corresponding directly to the function of device elements in claim 5. Therefore claim 24 is rejected as set forth above for claim 5.

Referring to claim 25:

Claim 25 is the method claim corresponding to operation of the device in claim 6 with method steps corresponding directly to the function of device elements in claim 6. Therefore claim 25 is rejected as set forth above for claim 6.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quang N. Vo whose telephone number is 5712701121. The examiner can normally be reached on 7:30AM-5:00PM Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, King Y. Poon can be reached on 5712727440. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you

have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Quang N. Vo/

Examiner, Art Unit 2625

/King Y. Poon/

Supervisory Patent Examiner, Art Unit 2625